ATTY DOCKET NO. SERIAL NO. 16877 unassigned INFORMATION DISCLOSURE CITATION TEIICHIRO NISHIZAKA (Use several sheets if necessary) **FILING GROUP** herewith unassigned **U.S. PATENT DOCUMENTS** *EXAMINER FILING DATE DOCUMENT NUMBER DATE NAME CLASS **SUBCLASS** INITIAL IF APPROPRIATE 6,399,441 **Ogura** 6/4/2002 6,388,293 5/14/02 Ogura, et al. 6,011,725 Eitan 1/4/00 6,256,231 7/3/01 Lavi, et al. FOREIGN PATENT DOCUMENTS **TRANSLATION** DOCUMENT NUMBER DATE COUNTRY CLASS **SUBCLASS** YES NO 2001-230332 8/24/01 Japan 2002-26149 Japan 1/25/02 Japan 2001-357681 12/26/01 Japan 2001-512290 8/21/01 2001-156189 6/8/01 Japan (Including Author, Title, Date, Pertinent Pages, Etc.) OTHER DOCUMENTS A Novel 2-bit/cell MONOS Memory Device with a Wrapped-Control-Gate Structure that Applies Source-Side Hot Electron Injection by Hideto Tomiye et al., 2002 Symposium on VLSI Technology Digest of a Technical papers, pp 206-207.

EXAMINER

DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

Form PTO-A820 (also form PTO-1449)

P09C/REV03

Patent and Trademark Office * U.S. DEPARTMENT OF COMMERCE

PATENTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Teiichiro Nishizaka

Docket: 16877

Serial No:

Unassigned

Art Unit: Unassigned

Filed:

Herewith

Dated: August 1, 2003

For:

NON-VOLATILE SEMICONDUCTOR

MEMORY DEVICE, METHOD FOR

MANUFACTURING SAME AND METHOD

FOR CONTROLLING SAME

Commissioner for Patents P. O. Box 1450 Alexandria, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

Sir:

In accordance with 37 C.F.R. §§ 1.97 and 1.98, it is requested that the following references, which are also listed on the attached Form PTO-1449, be made of record in the above-identified case.

1. "A Novel 2-bit/cell MONOS Memory Device with a Wrapped-Control-Gate Structure that Applies Source-Side Hot Electron Injection" by Hideto Tomiye et al., 2002 Symposium on VLSI Technology Digest of a Technical papers, pp 206-207.

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

"Express Mail" Mailing Label Number: EV-185-861-346-US Date of Deposit: August 1, 2003.

I hereby certify that this correspondence is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 C.F.R. § 1.10 on the date indicated above and is addressed to the Commissioner for Patents and Trademarks, Alexandria, VA 22313 on August 1, 2003.

Dated: August 1, 2003

Paul J. Esatto, Jr.

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- 2. Japanese Patent Application No. 2001-230332 dated August 24, 2001
- 3. Japanese Patent Application No. 2002-26149 dated January 25, 2002.
- 4. Japanese Patent Application No. 2001-357681 dated December 26, 2001.
- 5. U.S. Patent No. 6,399,441 issued to Ogura et al. dated June 4, 2002.
- 6. U.S. Patent No. 6,388,293 issued to Ogura et al. dated May 14, 2002.
- 7. Japanese Patent Application No. 2001-512290 dated August 21, 2001.
- 8. U.S. Patent No. 6,011,725 issued to Eitan dated January 4, 2000.
- 9. U.S. Patent No. 6,256,231 issued to Lavi et al. dated July 3, 2001.
- 10. Japanese Patent Application No. 2001-156189 dated June 8, 2001.

Applicant is submitting copies of the above-cited references, except the U.S. Patents, pursuant to the notice of waiver of 37 C.F.R. 1.98 (a) (2) published June 30, 2003. The relevance of the above-identified references has been described in the specification.

Inasmuch as this Information Disclosure Statement is being submitted in accordance with the schedule set out in 37 C.F.R. § 1.97(b), no statement or fee is required.

Respectfully submitted,

Paul J. Esatto, Jr.

Registration No.: 30,749

Scully, Scott, Murphy & Presser 400 Garden City Plaza Garden City, New York 11530 (516) 742-4343

PJE:eg